REMARKS

This Amendment responds to the Office Action dated September 15, 2003 in which the Examiner rejected claims 7, 9-10, 12 and 15-16 under 35 U.S.C. §102(e), stated that claim 18 is allowed and objected to claims 8, 11, 15-14 and 17 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, claim 7 has been amended to make explicit what is implicit in the claims. Furthermore, claim 8 has been rewritten into independent form and claims 9-10, 12 and 15-17 have been amended to correspond to claim 7. Applicants respectfully submit that the amendments are unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claims.

Claim 7 claims a method for manufacturing electronic devices obtained by equipping with electronic component chips on a printed circuit board and so forth. The method comprises the steps of: first, supplying a plurality of electronic component chips in an aligned relationship. The external electrodes of the electronic component chips are then cleaned.

Through the method of the claimed invention cleaning the external electrodes of the electronic component chips, as claimed in claim 7, the claimed invention provides a method of manufacturing electronic devices in which reliable electrical connection is provided. The prior art does not show, teach or suggest the invention as claimed in claim 7.

Claims 7, 9-10, 12 and 15-16 were rejected under 35 U.S.C. §102(e) as being anticipated by *Togawa et al.* (U.S. Patent No. 6,283,822).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(e). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allow the claims to issue.

Togawa et al. appears to disclose a polishing apparatus for polishing a workpiece such as a semiconductor wafer to a flat mirror finish. (col. 1, lines 9-11) The surfaces of semiconductor wafers are made flat for photolithography. One customary way of flattening the surfaces of semiconductor wafers is to polish them by a chemical mechanical polishing (CMP). (col. 1, lines 23-26) As shown in FIGS. 1 and 2, a polishing apparatus comprises a pair of polishing units 1a, 1b positioned at one end of a rectangular floor space and spaced from each other in confronting relation to each other, and a pair of loading/unloading units positioned at the other end of the rectangular floor space and having respective wafer storage cassettes 2a, 2b spaced from the polishing units 1a, 1b in confronting relation thereto. Two transfer robots 4a, 4b are movably mounted on a rail 3 which extends between the polishing units 1a, 1b and the loading/unloading units, thereby providing a transfer line along the rail 3. The polishing apparatus also has a pair of reversing units 5, 6 disposed one on each side of the transfer line and two pairs of cleaning units 7a, 7b and 8a, 8b disposed one pair on each side of the transfer line. The reversing unit 5 is positioned between the cleaning units 7a and 8a, and the reversing unit 6 is

positioned between the cleaning units 7b and 8b. Each of the reversing units 5, 6 serves to turn a semiconductor wafer over. (col. 3, lines 20-39) The polishing unit 1a or 1b operates as follows: The semiconductor wafer 20 is held on the lower surface of the top ring 13, and pressed against the polishing cloth 14 on the upper surface of the turntable 9. The turntable 9 and the top ring 13 are rotated relatively to each other for thereby bringing the lower surface of the semiconductor wafer 20 in sliding contact with the polishing cloth 14. At this time, the abrasive liquid nozzle 15 supplies the abrasive liquid to the polishing cloth 14. The lower surface of the semiconductor wafer 20 is now polished by a combination of a mechanical polishing action of abrasive grains in the abrasive liquid and a chemical polishing action of an alkaline solution in the abrasive liquid. The abrasive liquid which has been applied to polish the semiconductor wafer 20 is scattered outwardly off the turntable 9 into the frame 17 under centrifugal forces caused by the rotation of the turntable 9, and collected by the gutter 17a in the lower portion of the frame 17. The polishing process comes to an end when the semiconductor wafer 20 is polished by a predetermined thickness of a surface layer thereof. When the polishing process is finished, the polishing properties of the polishing cloth 14 is changed and the polishing performance of the polishing cloth 14 deteriorates. Therefore, the polishing cloth 14 is dressed to restore its polishing properties. (col. 4, lines 39-62)

Thus, *Togawa et al.* merely discloses a polishing apparatus for polishing a semiconductor wafer. Nothing in *Togawa et al.* shows, teaches or suggests a method of

manufacturing electronic devices. Rather, *Togawa* merely discloses a polishing apparatus for polishing a semiconductor wafer to a flat mirror finish.

Additionally, *Togawa et al.* merely discloses a polishing unit which polishes a semiconductor wafer 20. Nothing in *Togawa et al.* shows, teaches or suggests cleaning external electrodes of electronic component chips as claimed in claim 7. Rather, *Togawa* merely discloses polishing a semiconductor wafer.

Since nothing in *Togawa et al.* shows, teaches or suggests cleaning external electrodes of an electronic component chip or a method of manufacturing electronic devices as claimed in claim 7, Applicants respectfully request the Examiner withdraws the rejection to claim 7 under 35 U.S.C. §102(e).

Claim 9-10, 12 and 15-16 depend from claim 7 and recite additional features. Applicants respectfully submit that claims 9-10, 12 and 15-16 would not have been anticipated by *Togawa et al.* within the meaning of 35 U.S.C. §102(e) at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 9-10, 12 and 15-16 under 35 U.S.C. §102(e).

Claims 7, 9-10, 12 and 15-16 were rejected under 35 U.S.C. §102(e) as being anticipated by *Labunsky et al.* (U.S. Patent No. 6,132,289).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(e). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allow the claims to issue.

Labunsky et al. appears to disclose the field of semiconductor wafer processing and, more particularly, to equipment utilized to planarize semiconductor wafers. The manufacture of an integrated circuit device requires the formation of various layers above a base substrate to form the necessary components and interconnects. During the manufacturing process, removal of a certain layer or portions of a layer must be achieved in order to pattern and form various components and interconnects. In modern integrated circuit (IC) fabrication technology, it is necessary to form various structures over previous layers formed on a semiconductor wafer. With diminishing feature size such structures result in highly irregular surface topography causing manufacturing problems in the formation of thin film layers. To facilitate manufacturing processes, the rough surface topography has to be smoothened or planarized. One of the methods for achieving planarization of the wafer surface is chemical mechanical polishing (CMP). CMP is being extensively pursued to planarize a surface of a semiconductor wafer, such as a silicon wafer, at various stages of integrated circuit processing. CMP is also used in flattening optical surfaces, metrology samples, and various metal and semiconductor based substrates. (col. 1, lines 8-31) Referring to FIG. 1, a linear polisher 10 for use is shown. The linear polisher (also referred to as a linear planarization tool) 10 is utilized in planarizing a semiconductor wafer 11, such as a silicon wafer, to polish away materials on the surface of the wafer. The material being removed can be the substrate material of the wafer itself or one of the layers (such as a film layer) formed on the substrate. Formed layers include dielectric materials (such as silicon dioxide), metals (such as aluminum,

copper or tungsten) and alloys, or semiconductor materials (such as silicon or polysilicon). More specifically, a polishing technique generally known in the art as chemical-mechanical polishing (CMP) is employed to polish one or more of these layers fabricated on the wafer 11, in order to planarize the surface. Generally, the art of performing CMP to polish away layers on a wafer is known and prevalent practice has been to perform CMP by subjecting the surface of the wafer to a rotating platform (or platen) containing a pad (see for example, U.S. Pat. No. 5,329,732). The linear polisher 10 utilizes a belt 12, which moves linearly with respect to the surface of the wafer 11. The belt 12 is a continuous belt rotating about rollers (or spindles) 13 and 14, in which one roller or both is/are driven by a driving means, such as a motor, so that the rotational motion of the rollers 13-14 causes the belt 12 to be driven in a linear motion (as shown by arrow 16) with respect to the wafer 11. A polishing pad 15 is affixed onto the belt 12 at its outer surface facing the wafer 11. In some instances, the pad 15 and the belt 12 are integrated as a single unit. Either way, the belt/pad assembly is made to move linearly to planarize the wafer 11. (col. 4, lines 9-39) Adjacent to one side of the wet robot module 36 is a wet queue module 38 and on the opposite side is a scrubber/cleaner module 39. The wet queue module 38 provides for temporary storage of wafers which have undergone the polishing cycle, but are still waiting for cleaning performed by the scrubber/cleaner module 39. The scrubber/cleaner module 39 provides the final scrubbing and cleaning of the wafer after CMP has been performed. (col. 5, lines 44-51)

Thus, *Labunsky* merely discloses planarizing semiconductor wafers. Nothing in *Labunsky* shows, teaches or suggests a method of manufacturing electronic devices as claimed in claim 7. Rather, *Labunsky et al.* merely discloses planarizing semiconductor wafers.

Additionally, *Labunsky* merely discloses a linear polisher 10 which moves relative to a surface of a semiconductor wafer 11. Nothing in *Labunsky et al.* shows, teaches or suggests cleaning external electrodes of electronic component chips as claimed in claim 7. Rather, *Labunsky* merely discloses a linear polisher for polishing a wafer 11.

Since nothing in *Labunsky et al.* shows, teaches or suggests cleaning external electrodes of electronic component chips or a method for manufacturing electronic devices as claimed in claim 7, Applicants respectfully request the Examiner withdraws the rejection to claim 7 under 35 U.S.C. §102(e).

Claims 9-10, 12 and 15-16 depend from claim 7 and recite additional features. Applicants respectfully submit that claims 9-10, 12 and 15-16 would not have been anticipated within the meaning of 35 U.S.C. §102(e) by *Labunsky et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 9-10, 12 and 15-16 under 35 U.S.C. §102(e).

As indicated above, objected to claim 8 has been rewritten into independent form. Therefore, Applicants respectfully submit that the objection to claim 8 no longer applies. Furthermore, since claim 14 depends from claim 8, Applicants respectfully submit that this objection also no longer applies. Finally, since objected to claims 11, 13 and 17 depend

from an allowable claim, Applicants respectfully request the Examiner withdraws the objection thereto.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: December 11, 2003

By: _____
Ellen Marcie Emas
Registration No. 32,131

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620